REMARKS / DISCUSSION OF ISSUES

Claims 1-20 are pending in the application wherein claims 18-20 have been added. Claim 1 and 11 are independent.

The Office Action indicates that the oath or declaration is defective requiring a new oath or declaration since 37 CFR 1.56(a) is referred to instead of 37 CFR 1.56. A new oath or declaration is being concurrently filed.

The Office Action rejects claims 1-2, 4, 7-9 and 11-17 under 35 U.S.C. §103(a) over U.S. Patent No. 7,024,538 (Schlansker) in view of U.S. 6,076,159 (Fleck). Further, claims 3 and 5 are rejected under 35 U.S.C. §103(a) over Schlansker in view of Fleck and U.S. Patent Application Publication No. 2003/0145116 (Moroney). Claim 6 is rejected under 35 U.S.C. §103(a) over Schlansker in view of Fleck and Official Notice. Claim 10 is rejected under 35 U.S.C. §103(a) over Schlansker in view of Fleck and U.S. 5,208,781 (Matsushima). It is respectfully submitted that claims 1-20 are patentable over Schlansker, Fleck, Moroney, Official Notice, and Matsushima for at least the following reasons.

The Final Office Action correctly notes page 4 that Schlansker does not disclose or suggest to modify an address translation between supplying a first instruction address for a first instruction word and supplying a second instruction address for a second instruction word so that a part of the first instruction word is re-used in the second instruction word thereby reducing memory needed to store the program. Fleck is cited in an attempt to remedy the deficiencies in Schlansker.

Fleck is directed to a data processor having a first pipeline for decoding and executing data instructions, a second pipeline for decoding and executing address instructions, and a unit for issuing multiple instructions to the two pipelines that process data in parallel. Column 7, line 55 to column 8, line 9 disclose using loop operations in parallel.

It is respectfully submitted that Schlansker, Fleck, and combination thereof, do not teach or suggest the present invention as recited in independent claim 1, and

similarly recited in independent claim 11 which, amongst other patentable elements, recites (illustrative emphasis provided):

> an instruction address modification circuit arranged to modify translation of the instruction address into a physical address for a particular one of the memory units relative to other ones of the memory units and to change generation of instruction words from instructions from different memory units during execution of a program, the instruction address modification circuit being configured to modify an address translation between supplying a first instruction address for a first instruction word and supplying a second instruction address for a second instruction word, the second instruction word being different from the first instruction word and including a copy of a part of the first instruction word, so that the part of the first instruction word is re-used in the second instruction word thereby reducing memory needed to store the program,
>
> wherein the instruction address modification circuit includes **an offset register connected to an output of a functional unit** of the plurality of functional units, the functional unit updating an offset value in the offset register during the execution of the program.

An offset register connected to an output of a functional unit that updates an offset value in the offset register during the execution of the program is nowhere disclosed or suggested in Schlansker and Fleck, alone or in combination. Rather, Fleck merely discloses on column 8, lines 1-9 to compare a loop detection address with current program counter, and on subsequent loop iterations, a loop instruction is detected and executed, where a maximum of three instructions can be executed at the same time, while executing loops. Moroney, Official Notice, and Matsushima are cited to allegedly show other features and do not remedy the deficiencies in Schlansker and Fleck.

Accordingly, it is respectfully submitted that independent claims 1 and 11 are allowable. In addition, claims 2-10 and 12-120 are allowable at least because they depend from independent claims 1 and 11, as well as for the separately patentable elements contained in each of the dependent claims.

In addition, Applicants deny any statement, position or averment of the Examiner that is not specifically addressed by the foregoing argument and response. Any rejections and/or points of argument not addressed would appear to be moot in view of the presented remarks. However, the Applicants reserve the right to submit further arguments in support of the above stated position, should that become necessary. No arguments are waived and none of the Examiner's statements are conceded. And in particular, no Official Notices are conceded.

In view of the foregoing, applicants respectfully request that the Examiner withdraw the objection(s) and/or rejection(s) of record, allow all the pending claims, and find the application in condition for allowance. If any points remain in issue that may best be resolved through a personal or telephonic interview, the Examiner is respectfully requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Dicran Halajian
Reg. 39,703
Attorney for Applicant(s)
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THORNE & HALAJIAN, LLP
Applied Technology Center
111 West Main Street
Phone: (631) 665-5139
Fax: (631) 665-5101